

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,822,925 B2
DATED : November 23, 2004
INVENTOR(S) : Scott Van De Graaff

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12,

Line 30, "1126, and control signal 11O buffers 1124. Interconnect lines" should read -- 1126, and control signal I/O buffers 1124. Interconnect lines --.

Column 13,

Line 13, "delaying the second input clock signal the first lime period" should read -- delaying the second input clock signal the first time period --.

Column 14,


Line 46, "a first delay segment coupled o the clock input buffer," should read -- a first delay segment coupled to the clock input buffer, --.

Column 15,

Line 12, "circuit, the clock input buffer, and o a second delay" should read -- circuit, the clock input buffer, and a second delay --.

Signed and Sealed this

Twenty-eighth Day of March, 2006

A handwritten signature in black ink, appearing to read "Jon W. Dudas", is written over a faint, circular embossed seal of the United States Patent and Trademark Office.

JON W. DUDAS
Director of the United States Patent and Trademark Office